IN THE CLAIMS

The currently pending claims are as follows:

1-5. (Canceled)

6. (Previously Presented) A method comprising configuring a plurality of processing elements within a heterogeneous configurable circuit to demultiplex a data stream, operate on portions of the data stream in parallel, and multiplex results to a second data stream;

wherein configuring a plurality of processing elements further comprises configuring at least one programmable element to demultiplex the data stream into overlapping segments.

7. (Original) The method of claim 6 wherein the overlapping segments comprise data packets.

8. (Original) The method of claim 7 wherein configuring at least one programmable element comprises configuring the at least one programmable element to route data packets to a plurality of processing elements capable of filtering data.

9. (Previously Presented) A method comprising configuring a heterogeneous configurable device to:

demultiplex a packet-based input data stream into a plurality of separate overlapping data streams;

route the plurality of separate data streams to processing elements in parallel; and

multiplex output packets from processing elements in parallel to produce a packet-based output data stream.

10. (Original) The method of claim 9 wherein configuring the heterogeneous configurable device to demultiplex a packet-based input stream comprises configuring a programmable element that is coupled to routers in a row and column arrangement.

11. (Original) The method of claim 9 wherein configuring the heterogeneous configurable device to route the plurality of separate data streams comprises configuring a programmable element that is coupled to routers in a row and column arrangement.

12. (Original) The method of claim 9 wherein configuring the heterogeneous configurable device to multiplex output packets from processing elements in parallel comprises configuring a programmable element that is coupled to routers in a row and column arrangement.

13. (Original) The method of claim 9 wherein configuring the heterogeneous configurable device to route the plurality of separate data streams comprises configuring a programmable element to route the separate data streams to a plurality of processing elements capable of filtering data.

14. (Original) The method of claim 13 wherein filtering data comprises performing a Fast Fourier Transform.

15. (Original) The method of claim 13 wherein filtering data comprises performing a finite impulse response filter.

16. (Original) The method of claim 9 wherein configuring the heterogeneous configurable device to route the plurality of separate data streams comprises configuring a programmable element to route the separate data streams to a plurality of processing elements capable of implementing a Viterbi decoder.

17. (Previously Presented) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

configuring a plurality of processing elements within a heterogeneous configurable circuit to demultiplex a packet-based data stream into a plurality of overlapping data streams, operate on the plurality of overlapping data streams in parallel, and multiplex results to a second data stream.

18. (Original) The apparatus of claim 17 wherein configuring a plurality of processing elements comprises configuring a plurality of processing elements capable of filtering data.

19. (Original) The apparatus of claim 18 wherein configuring a plurality of processing elements further comprises configuring at least one router to route data packets within the integrated circuit.

20. (Previously Presented) An apparatus comprising:

a heterogeneous plurality of configurable processing elements; and

a plurality of interconnected routers to route packets between the plurality of configurable processing elements;

wherein a subset of the plurality of configurable processing elements are configurable to operate on a plurality of overlapping data sub-streams in parallel.

21. (Previously Presented) The apparatus of claim 20 wherein the plurality of interconnected routers are configurable to demultiplex a data stream to produce the plurality of overlapping data sub-streams.

22. (Previously Presented) The apparatus of claim 21 wherein the plurality of interconnected routers are further configurable to route the plurality of overlapping data sub-streams to the subset of the plurality of configurable processing elements.

23. (Previously Presented) The apparatus of claim 20 wherein at least one of the plurality of configurable processing elements is configurable to demultiplex a data stream to produce the plurality of overlapping data sub-streams.

24. (Previously Presented) The apparatus of claim 23 wherein the at least one of the plurality of configurable processing elements are further configurable to route the plurality of overlapping data sub-streams to the subset of the plurality of configurable processing elements.

25. (Original) The apparatus of claim 20 wherein the subset of the plurality of configurable processing elements comprises micro-coded processing elements.

26. (Original) The apparatus of claim 25 wherein the micro-coded processing elements comprise filter micro-coded accelerators.

27. (Previously Presented) An electronic system comprising:

an antenna;

a radio frequency circuit to receive communications signals from the antenna; and

a configurable circuit coupled to the radio frequency circuit, the configurable circuit including a heterogeneous plurality of configurable processing elements, and a plurality of interconnected routers to route packets between the plurality of configurable processing elements, wherein a subset of the plurality of configurable processing elements are configurable to operate on a plurality of overlapping data sub-streams in parallel.

28. (Previously Presented) The electronic system of claim 27 wherein at least one of the plurality of configurable processing elements are configurable to demultiplex a data stream to produce the plurality of overlapping data sub-streams.

29. (Original) The electronic system of claim 27 wherein the subset of the plurality of configurable processing elements are configurable to perform a Fast Fourier Transform.

30. (Original) The electronic system of claim 27 wherein the subset of the plurality of configurable processing elements are configurable to perform a finite impulse response filter.